

A

**In the Specification:**

Please replace the paragraph beginning at Page 18, line 27 with the following paragraph:

**Figure 8F** illustrates the formation and patterning of the gate oxide 28. The gate oxide is preferably thermally grown and is a nitrided oxide. The nitrided oxide may be any suitable gate oxide, however, SiO<sub>2</sub>, oxynitride or ONO may be preferred. Formation of the gate oxide or the initial oxide of an ONO gate dielectric is preferably followed by an anneal in N<sub>2</sub>O or NO so as to reduce defect density at the SiC/oxide interface. In particular embodiments, the gate oxide is formed either by thermal growth or deposition and then annealed in an N<sub>2</sub>O environment at a temperature of greater than about 1100 °C and flow rates of from about 2 to about 8 SLM which may provide initial residence times of the N<sub>2</sub>O of from about 11 to about 45 seconds. Such formation and annealing of an oxide layer on silicon carbide are described in commonly assigned United States Patent Application Serial No. 09/834,283, entitled "Method of N<sub>2</sub>O Annealing an Oxide Layer on a Silicon Carbide Layer" (Attorney Docket No. 5308-15[6]7) or as described in United States Provisional Application Serial No. [ ]60/294,307 entitled "Method of N<sub>2</sub>O Growth of an oxide layer on a Silicon Carbide Layer" filed May 30, 2001, the disclosures of which are incorporated herein by reference as if set forth fully herein. Additionally, an N<sub>2</sub>O grown oxide may also be utilized as described in J. P. Xu, P. T. Lai, C. L. Chan, B. Li, and Y. C. Cheng, "Improved Performance and Reliability of N<sub>2</sub>O-Grown Oxynitride on 6H-SiC," IEEE Electron Device Letters, Vol. 21, No. 6, pp. 298-300, June 2000. Techniques as described in L. A. Lipkin and J. W. Palmour, "Low interface state density oxides on p-type SiC," Materials Science Forum Vols. 264-268, pp. 853-856, 1998 may also be utilized. Alternatively, for thermally grown oxides, a subsequent NO anneal of the thermally grown SiO<sub>2</sub> layer may be provided to reduce the interface trap density as is described in M. K. Das, L. A. Lipkin, J. W. Palmour, G. Y. Chung, J. R. Williams, K. McDonald, and L. C. Feldman, "High Mobility 4H-SiC Inversion Mode MOSFETs Using Thermally Grown, NO Annealed SiO<sub>2</sub>," IEEE Device Research Conference, Denver, CO, June 19-21, 2000; G. Y. Chung, C. C. Tin, J. R.